

A square root extraction circuit and a floating-point square root extraction device which simplify a circuit structure and improve an operation speed are provided. Portions for generating square root partial data ( $q_3$  to  $q_8$ ) include carry output prediction circuits (3 to 8), respectively. The carry output prediction circuit (i) (i equals any one of 3 to 8) receives condition flags (AHin, ALin), the most significant addition result (SUM), and square root partial data ( $q_{(i-1)}$ ) from the preceding square root partial data generating portion, and also receives a carry input (Cin) to output condition flags (AHout, ALout) for the next square root partial data generating portion, and square root partial data ( $q_{(i)}$ ). The condition flags (AHout, ALout) serve as the condition flags (AHin, ALin) for the carry output prediction circuit (i+1), respectively.